

Fig. 1
Prior Art

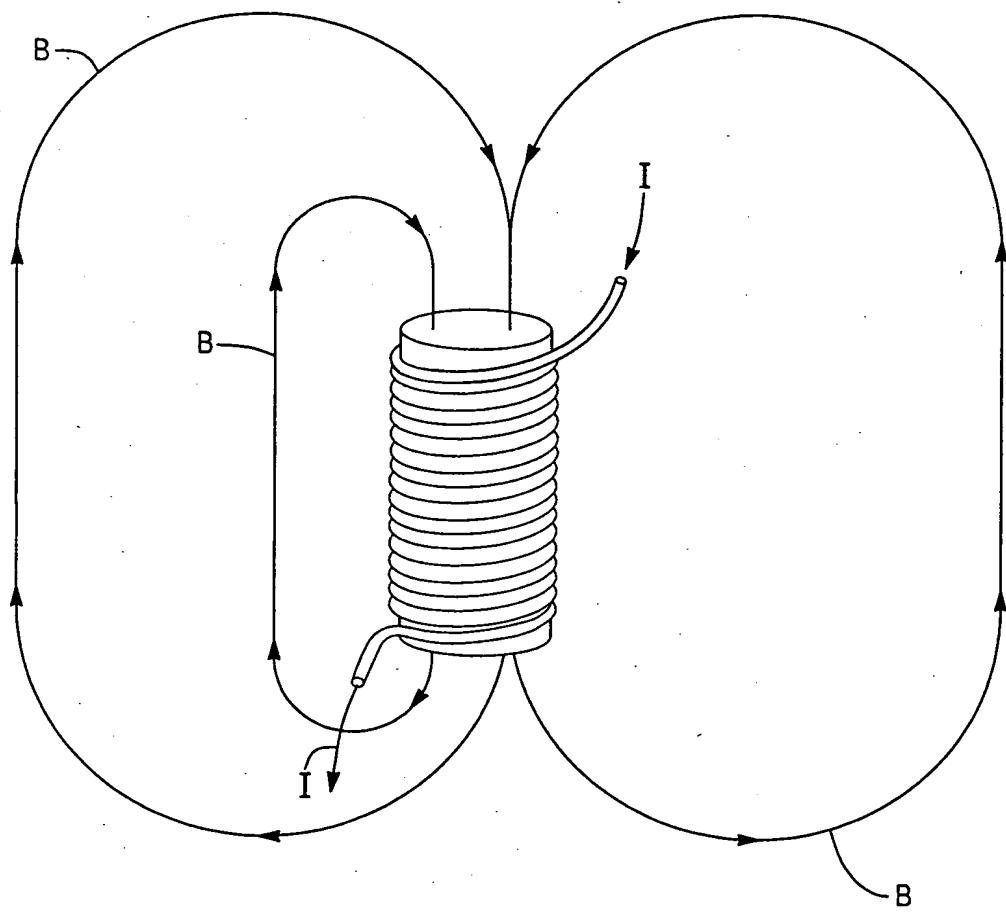


Fig. 2

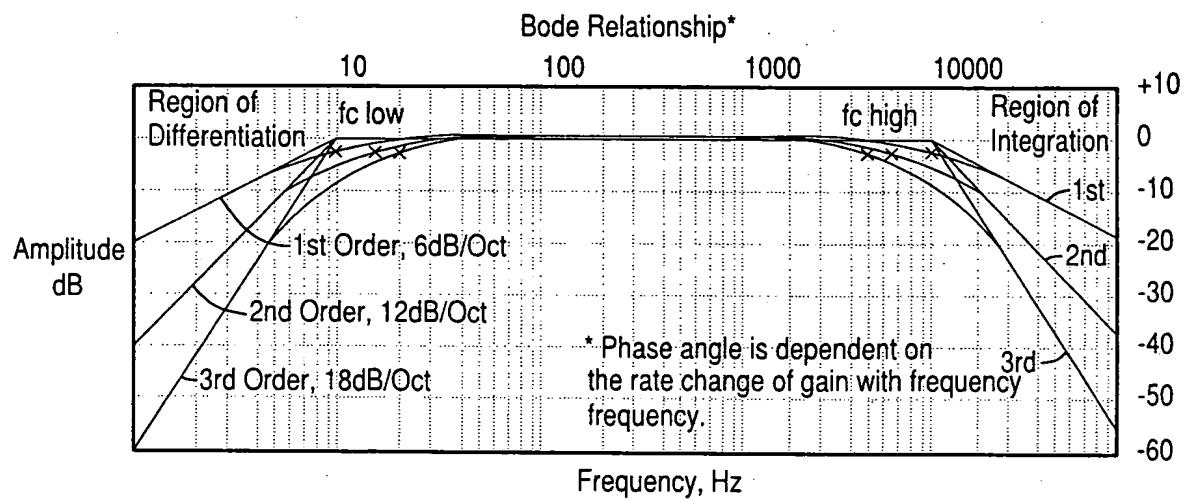
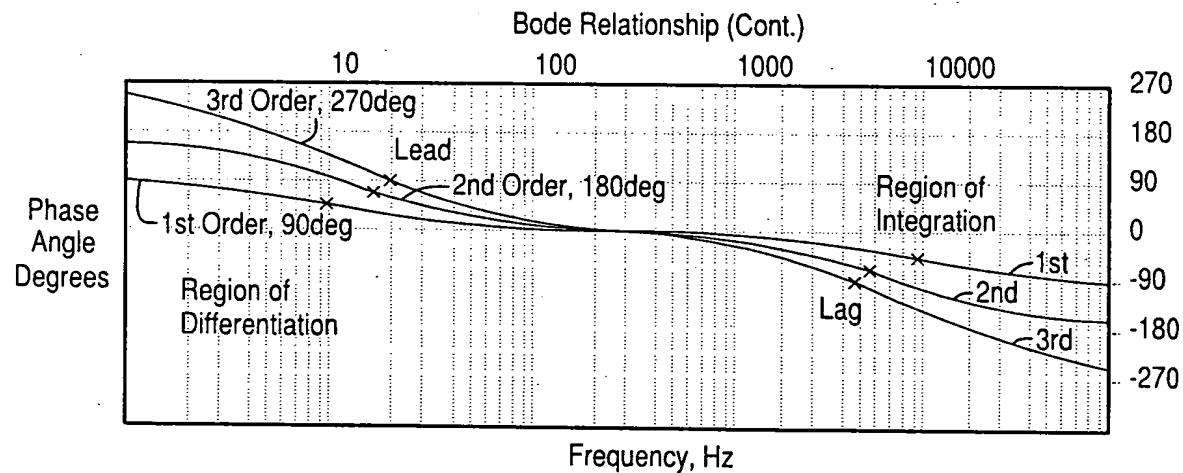


Fig. 3



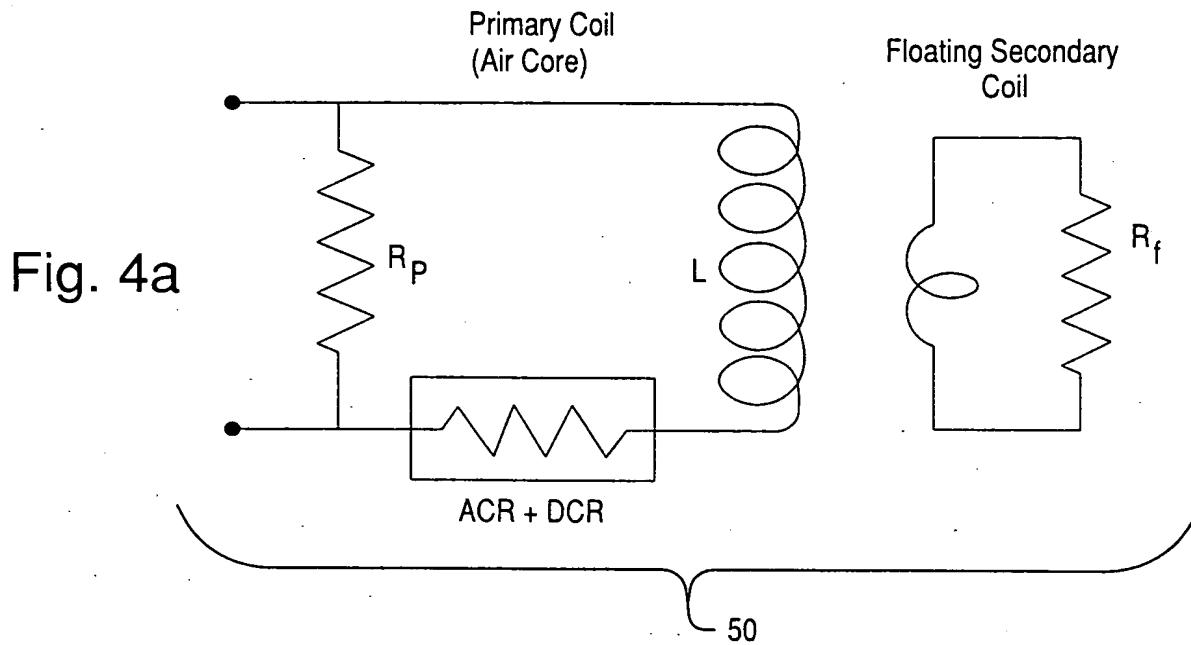


Fig. 4b

Equivalent Circuit

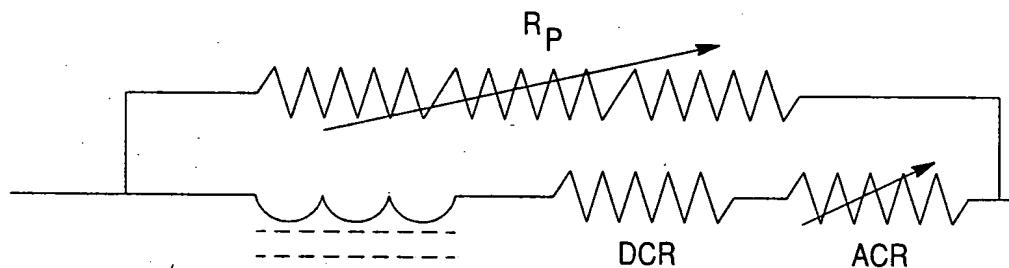


Fig. 4c

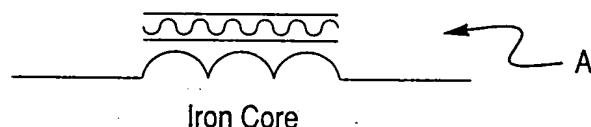


Fig. 4d

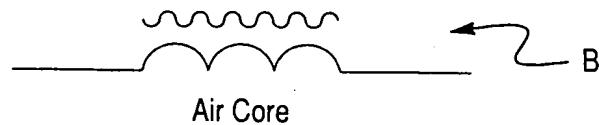


Fig. 5

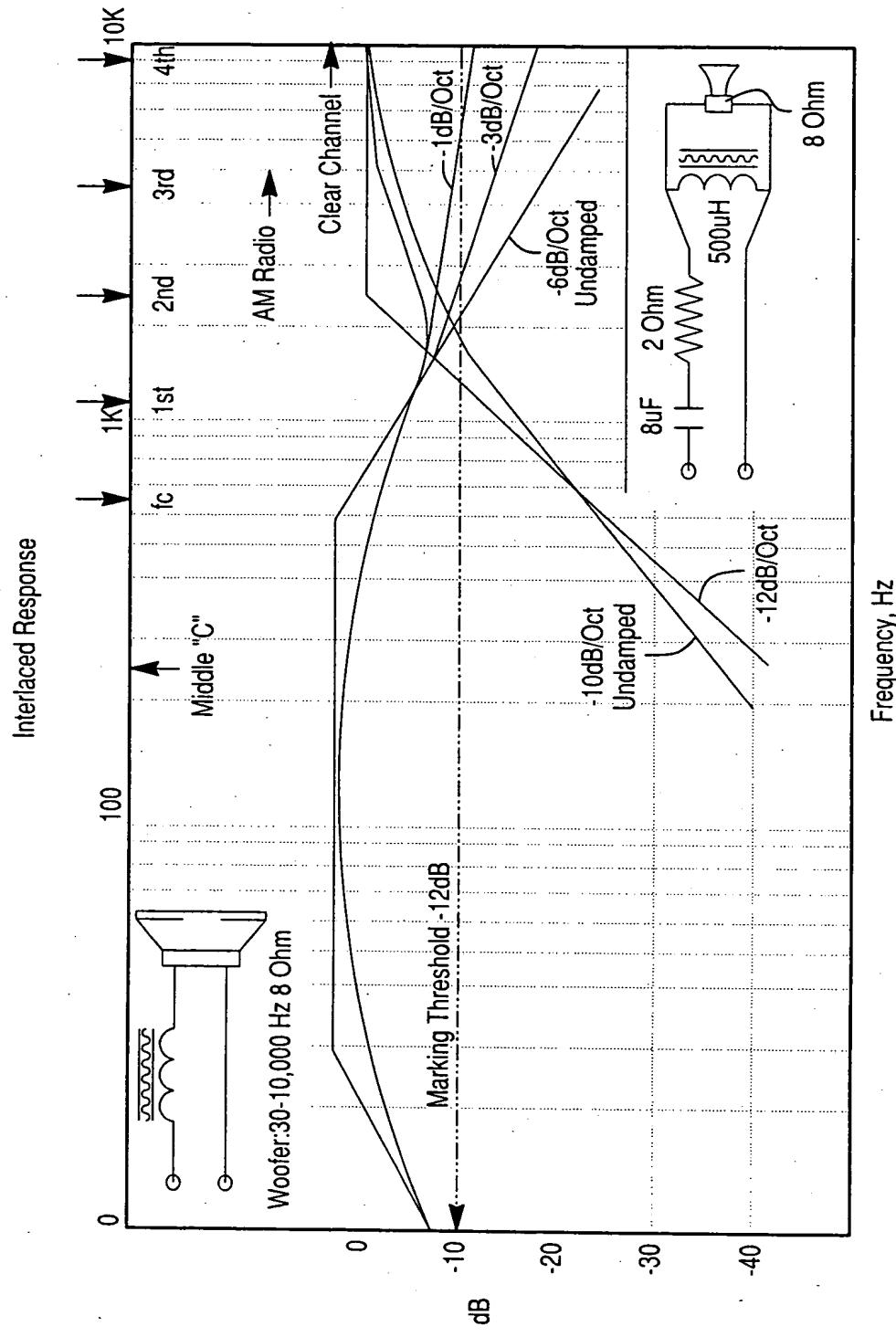


Fig. 6

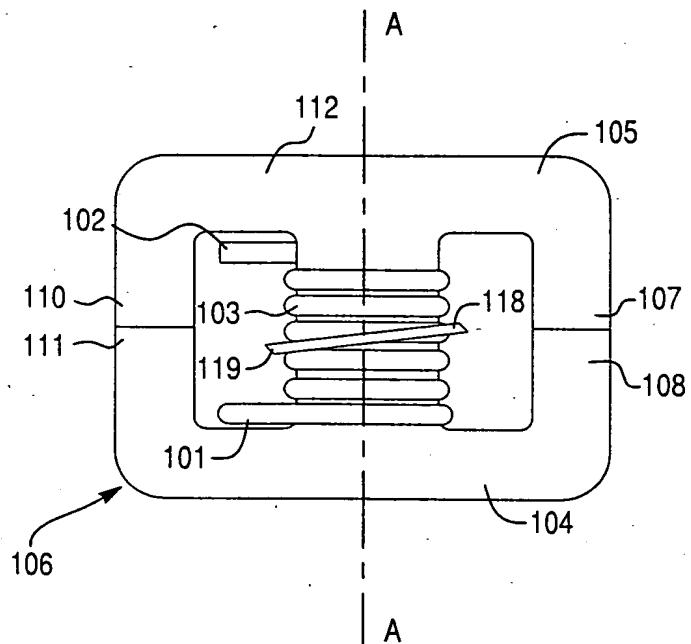


Fig. 7

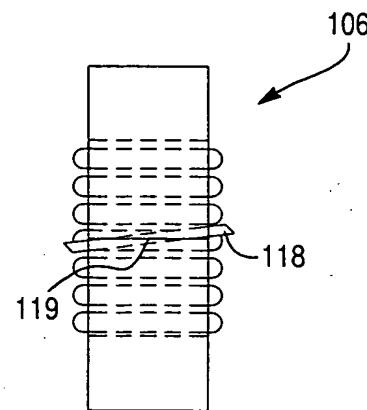


Fig. 8

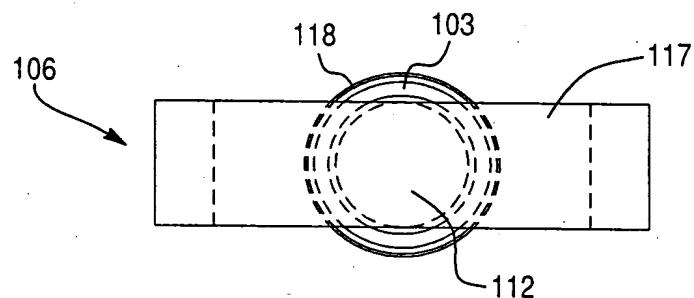


Fig. 9

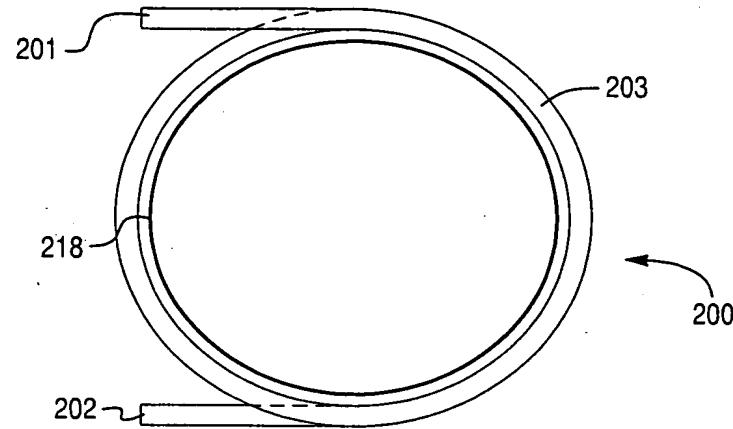


Fig. 10

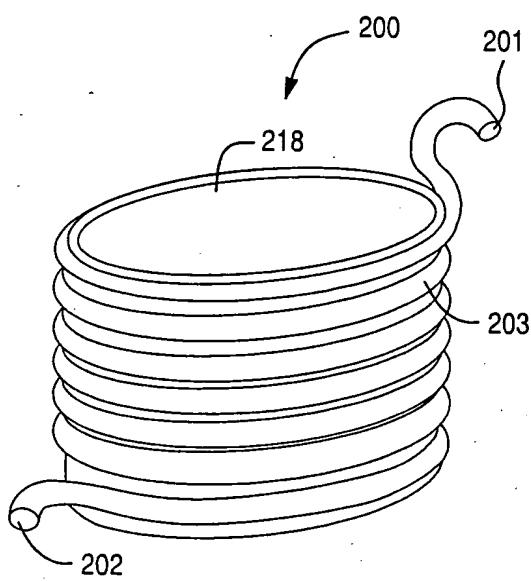


Fig. 11

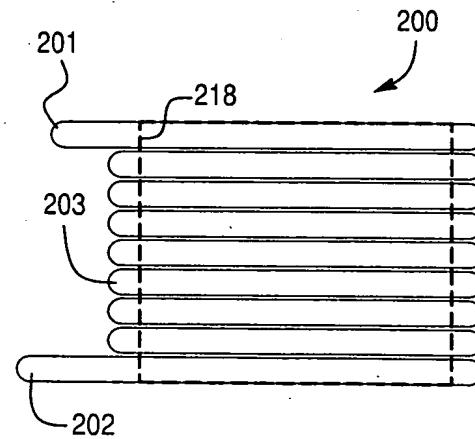


Fig. 12

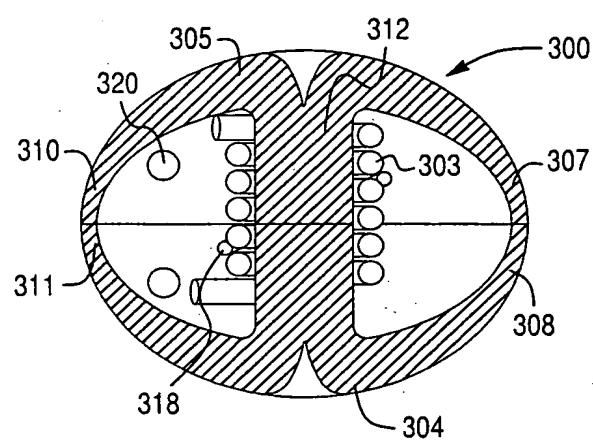


Fig. 13

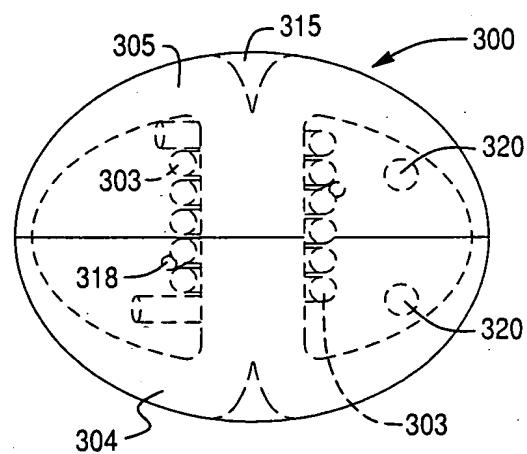


Fig. 14

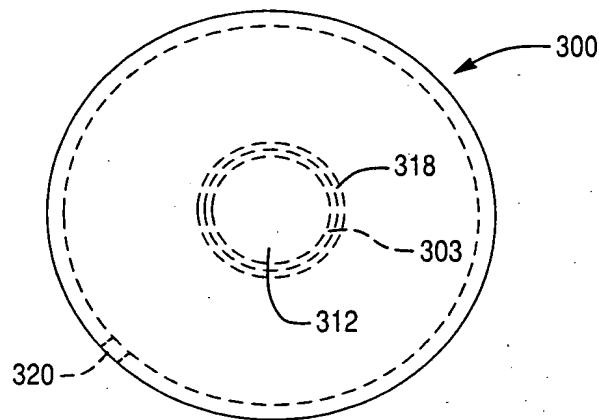


Fig. 15

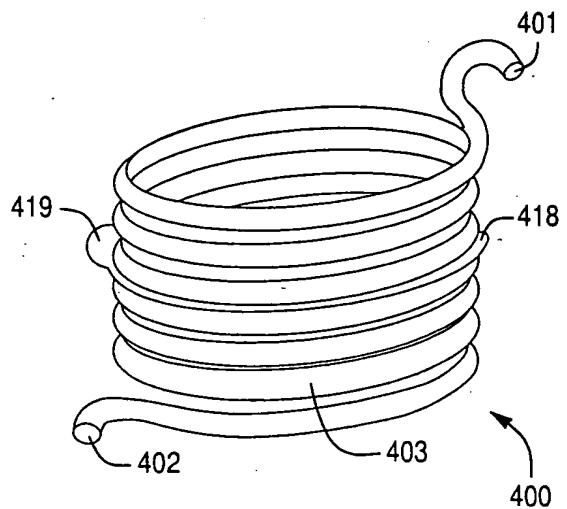


Fig. 16

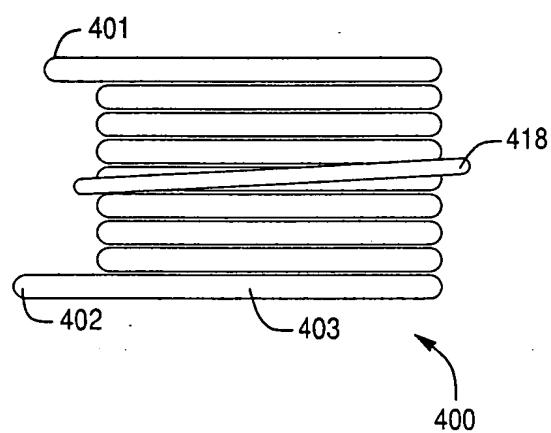


Fig. 17

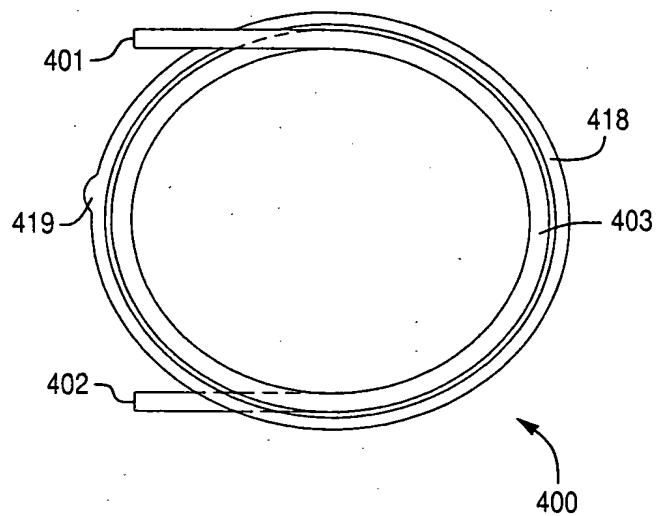


Fig. 18

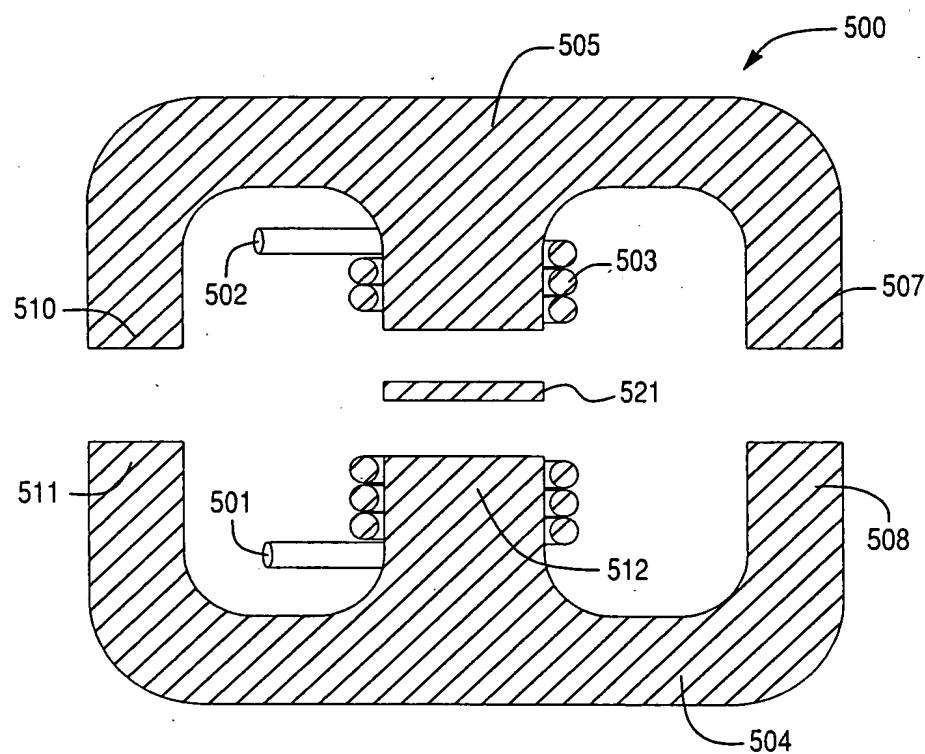


Fig. 19

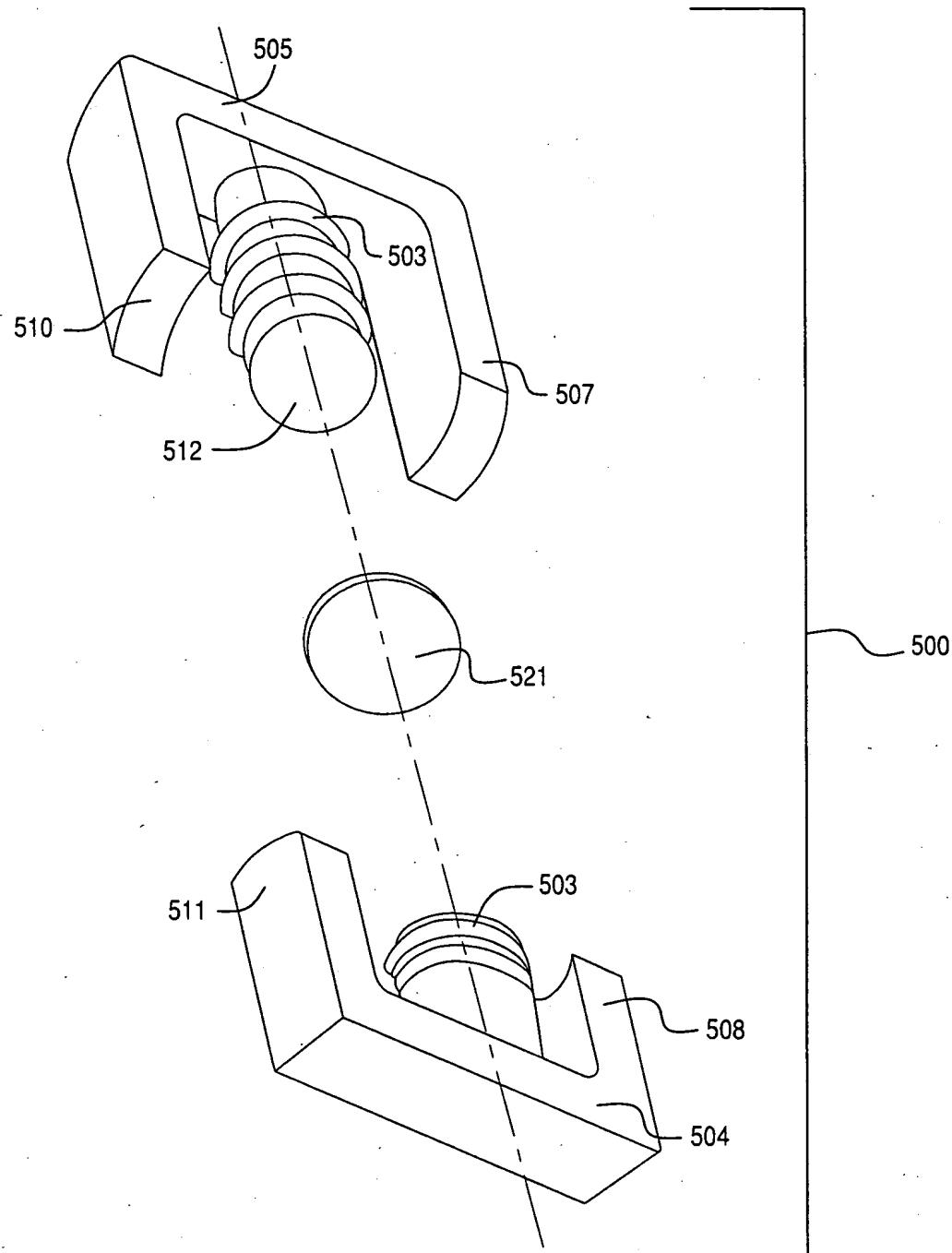


Fig. 20

